DESIGN OF A HIGH PERFORMANCE SERIAL SERIAL MULTIPLIER

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ABSTRACT

In the past few years, multipliers have been a tremendous increase in the demand for better quality electronic equipment because of increasing standards of living of people. This has led to the development of new technologies like System On Chip (S.O.C)s and scaling down the transistor sizes so that we can integrate a greater amount of functionality into a smaller area of silicon.

The densely packed components will result in higher power consumption per unit area of silicon and higher power dissipation too. This could result in increasing the temperature of the chip which could slow down the chip or could damage it. The higher power consumption also leads to quick draining of battery operated devices. In many palm-hold devices like smart phones, i-pods etc there are many applications like voice interface, high definition audio and video, video calling, 3G and 4G services, etc. which needs a very good quality DSP circuit.FIR Filters are a major component of DSP circuits. FIR Filters mainly comprise of multipliers and adders as the power consuming elements. For a good quality DSP circuit we need to implement an FIR Filter with wide multipliers that give good precision and range for good multiplication. And also some times to reduce the wiring cost, it is common practice to transmit the data through a high speed serial link. In some ICs the designers try to reduce the number of IO pads in order to reduce the power consumption and silicon area. Therefore efforts are made to design high speed serial interface in order to facilitate on-chip buffering and parallel processing. In this project we design seral-serial multiplier to reduce the complexity of SOC's, and power dissipation. The RTL coding for this project has been done in verilog HDL. Modelsim Simulator has been used to perform functional verification through simulation. XILINX ISE is used to perform synthesis and power analysis.

KEYWORDS: Binary Multiplication, Parallel Multipliers, Serial Multipliers, On-Chip Serial Link Bus Architecture